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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,229	12/20/2001	Grzegorz J. Pakulski	13149-003001 / 14404RO	9027
26161	7590	10/24/2003	EXAMINER	
FISH & RICHARDSON PC 225 FRANKLIN ST BOSTON, MA 02110			VY, HUNG T	
			ART UNIT	PAPER NUMBER
			2828	

DATE MAILED: 10/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/027,229

Applicant(s)

PAKULSKI ET AL.

Examiner

Hung T Vy

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.


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Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other:

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DETAILED ACTION

1. In response to the communications dated 12/20/2001, claims 1-14 are pending in this application.

Specification

2. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings are objected to for the following reasons.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the figures 2-5 must be shown the feature(s) canceled from the claim(s). The claims recite p-n-p or n-p-n-p layers but not support on Figs. No new matter should be entered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1 is confusing, vague, and indefinite. For example, claim 1 recites only step of fabricating a hybrid current confinement region adjacent to active layer of the device without any support fabricating a hybrid current confinement region. Further, the claim recites disposing a sequence of the p-n-p layers and disposing a semi-insulating material without reciting how a sequence of the p-n-p layers fabricating surrounding the active layers and how semi-insulating material fabricating around the p-n-p surrounding the active layers. Claim 1 is not supported by any figures in application. The figs. 2-5 show the n-p or p-n layer (not p-n-p as claim).

Regarding claim 10 is confusing, vague, and indefinite. For example, the claim recites a semiconductor substrate supporting an active region, confinement layers comprising: a sequence of doped n-p-n-p semiconductor layer and a semi-insulating semiconductor without reciting the structure relation between those element in order to form a semiconductor device. Where are the active region, confinement layers in the semiconductor device? Further, Claim 10 is not supported by any figures in application. The figs. 2-5 show the n-p or p-n layer (not n-p-n-p as claim).

Claims 2-9, and 11-14 depend from rejected claim 1 and 10 thereby render these dependent claims indefinite.

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The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

35 U.S.C. § 102(e), as revised by the AIPA and H.R. 2215, applies to all qualifying references, except when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. For such patents, the prior art date is determined under 35 U.S.C. § 102(e) as it existed prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. § 102(e)).

5. Claims 1-2, 4-11 and 13-14 are rejected under 35 U. S. C. § 102 (e) as being anticipated by Jie et al., U.S. patent No. 6,287,884.

Regarding claims 1-2,4-6 and 10, Jie et al. discloses a method of fabricating and a semiconductor device comprising: a semiconductor substrate supporting an active region (4) comprised of a multiple quantum well active regions (see column 5, line 29-30) and confinement layers having defined gratings and grating overgrowth regions to produce a laser device (see fig 1); and a current confinement layer (8,9) comprising: a sequence of doped n-p-n-p semiconductor layers (8,9) to produce a n-p-n-p blocking structure(8,9); and semi-insulating semiconductor (13) material adjacent to the etched n-p-n-p blocking structure (See fig.1), depositing a doped p type layer as capping layer (6) over the mesa to provide the n-p-n-p current blocking structure (see column 4, line 37 and fig. 1).

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Regarding claims 7-9, Jie et al. discloses the method of fabricating a buried heterostructure semiconductor device, wherein producing further comprises; etching away portions (12) of the n-p-n-p current blocking structure using a wide oxide mask disposed over the capping layer (See fig. 1), re-growing semi-insulating semiconductor material over the etched n-p-n-p blocking structure (13)(See fig 1h), and providing contact metalization on the semiconductor contact layers (14)(See fig 1).

Regarding claims 13-14, Jie et al. discloses the semiconductor device, wherein the semiconductor substrate material is n-type doped InP (see column 5, line 21-24) and p-type contact (11) material InGaAs (See column 4, line 48).

6. Claims 1-14 are rejected under 35 U. S. C. § 102 (b) as being anticipated by Kimura et al., U.S. patent No. 5, 452,315.

Regarding claims 1-14, Kimura et al. discloses a method of fabricating and a semiconductor device comprising: a semiconductor substrate supporting an active region (2) comprised of a multiple quantum well active regions (See fig. 1) and confinement layers having defined gratings and grating overgrowth regions to produce a laser device (see fig 1); and a current confinement layer (4,6) comprising: a sequence of doped n-p-n-p semiconductor layers (4,6) to produce a n-p-n-p blocking structure (4,6); and semi-insulating semiconductor (5) material adjacent to the etched n-p-n-p blocking structure (See fig.1), depositing a doped p type layer as capping layer (3a) over the mesa to provide the n-p-n-p current blocking structure (see fig. 1-17).

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Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, and 12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Jie et al., U.S. patent No. 6,287,884 in view of Weber, U.S. Patent No. 6,421,492.

Regarding claims 3, and 12, Jie et al. discloses all limitation of claim except the semi-insulating material is InP doped with Fe. However, Weber discloses the semi-insulating material is InP doped with Fe to provide current confinement for current generated in the active layer (See column 2, line 43-47). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify Jie et al. to have the semi-insulating material is InP doped with Fe as taught by Weber because those skilled in the art will recognize that such modification and variations can be made without departing from the spirit of the invention.

Citation of Pertinent References

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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The patent to Swirhun et al. discloses Integration of Laser with photodiode for Feedback Control, U.S. Patent No. 5,606,572.

The patent to Yokoyama et al. discloses Semiconductor Photonic Element, Method of Fabricating the Same, and Semiconductor Photonic Device Equipped Therewith, U.S. Patent No. 6,323,507.

Conclusion

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung Vy whose telephone number is (703) 605-0759. The examiner can normally be reached on Monday-Friday 8:30 am - 5:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul IP can be reached on (703) 308-3098. The fax numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



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Hung T. Vy

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October 14, 2003